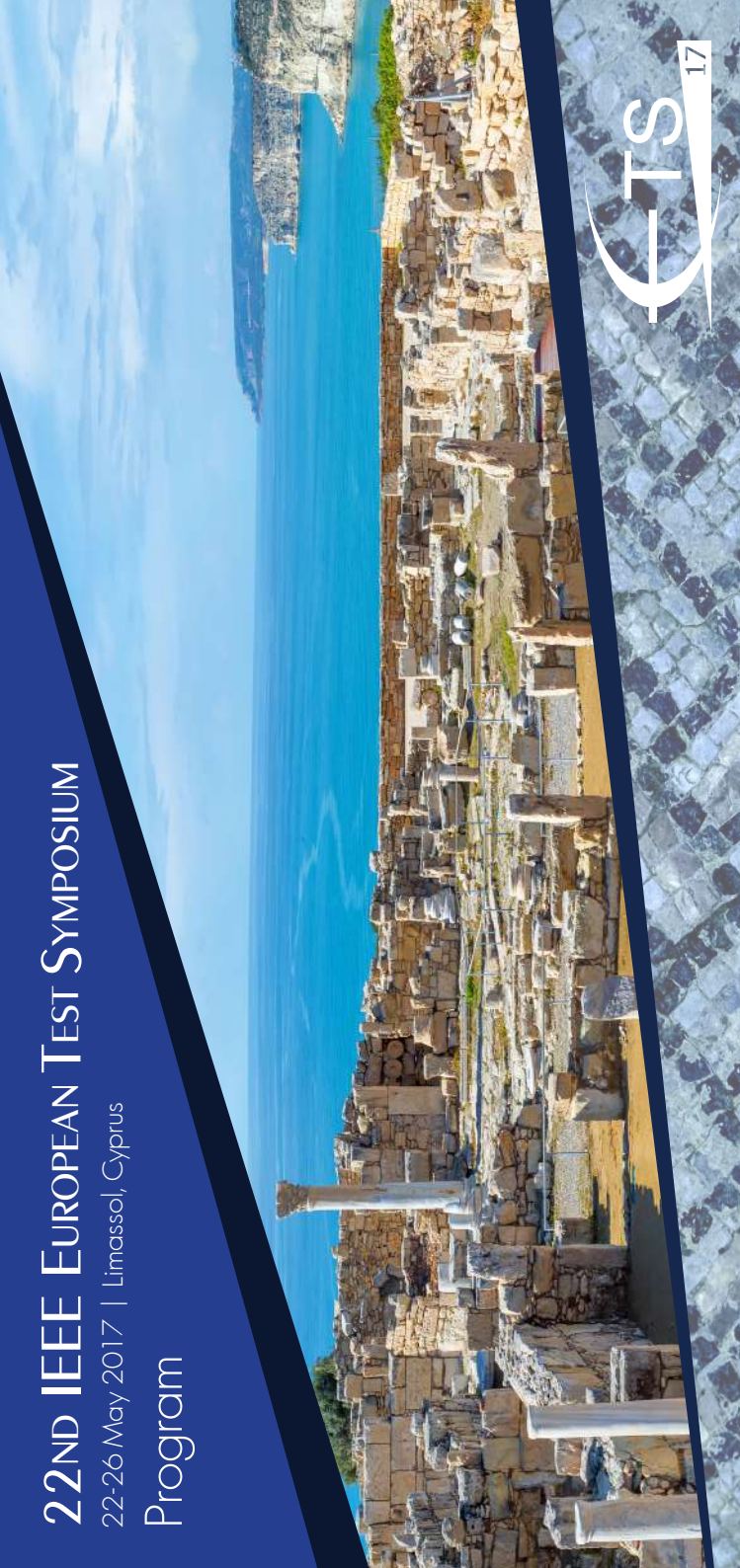


# 22ND IEEE EUROPEAN TEST SYMPOSIUM

22-26 May 2017 | Limassol, Cyprus

Program



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On behalf of the Program, Organizing, and Steering Committees, we would like to extend a warm welcome to everyone attending the European Test Symposium 2017 (ETS'17). ETS has been established as one of the main international forums and the larger forum in Europe that brings together the test community to discuss emerging ideas, views, and trends in the area of electronic-based circuits and system testing. Topics of interest include, but are not limited to, design-for-test, dependability, security, failure analysis and diagnosis, on-line test, automated test hardware, validation and verification, fault simulation, fault tolerance, automatic test generation, etc.

This year ETS takes place in Limassol, Cyprus and is organized by the University of Cyprus, which co-sponsors the event jointly with the IEEE Council on Electronic Design Automation (CEDA). The coastal city of Limassol is the island's second largest city and it spreads out between two ancient city-kingdoms, Amathous (1100 BC) to the east and Kourion (4500 BC) to the west, two of the most spectacular archaeological sites in Cyprus. Limassol is a multifaceted city, being the main port of Cyprus; one of the most important trade and service-providing hubs in the region; the center of the country's wine industry; and a bustling holiday resort with a vibrant old town district.

ETS is the cornerstone event of the European Test Week, which includes in addition the Test Spring School (TTS) and Fringe Workshops. The topic for this year's TSS, which precedes the symposium, places the emphasis on Machine Learning for Test, Dependability and Fault Tolerance. Two Fringe Workshops will take place immediately following ETS'17, namely the 2<sup>nd</sup> International Test Standards Application (TESTA) Workshop, which focuses on test standards, and the 1st Workshop on Reliability, Security and Quality (RESCUE), which brings together the security community with the reliability, testing and verification communities to encourage fruitful discussions.

ETS'17 received a large number of scientific paper submissions from 23 countries spanning all continents except Antarctica and Australia. Each paper received on average 7 expert reviews. Based on the written reviews and follow-up online discussions among the reviewers, the Organizing Committee and the Topic Chairs convened in Athens, Greece, on February 3<sup>rd</sup>, 2017, and recommended to accept 19 papers for oral presentation, distributed over 8 regular sessions, and 19 papers for poster presentation, distributed over 3 one-hour sessions.

An Award Committee has been formed and will select the best paper based on the reviewers' comments and the ratings provided by the attendees. The authors of the best paper will receive the Best Paper Award during the opening ceremony of ETS'18.

During the meeting in Athens, all other aspects of the ETS'17 program were also discussed. Apart from scientific paper presentations, the ETS'17 program consists of 3 plenary keynote addresses, 4 one-hour embedded tutorials and 2 TSS@ETS Monday tutorials, 2 "wine-and-cheese" panel sessions, 3 special sessions, 3 vendor sessions, and several table-top demo presentations. In addition, ETS features for the fourth consecutive year a special track on Emerging Test Strategies (ETS<sup>2</sup>) where new issues are presented by the industry and are discussed in an informal atmosphere, as well as the new initiative of Industry Wish List where industry experts give elevator talks on open and challenging problems and call the test community to work on developing effective solutions.

Finally, the ETS'17 program is enriched with an exciting social program providing lots and superb opportunities for informal discussions among participants in a relaxed setting. Social activities start with a welcome reception offering sunset panoramic sea views of the Limassol shore. They continue with the main social event and include a sightseeing visit and cocktail party at the Kourion Archeological Site, followed by a gala dinner at the Evagoras Lanitis Centre - Carob Mill cultural center, which is situated in the old town of Limassol.

ETS'17 is the result of the hard work of many dedicated volunteers involved in the technical and organizational activities leading to the European Test Week. We wholeheartedly thank all of them for their significant effort to put together this edition of ETS. We also thank all authors who submitted their work to ETS'17, the presenters for their contributions, and all attendees for their active participation. We also thank the IEEE Council on Electronic Design Automation and the IEEE Computer Society Test Technology Technical Council for the continued technical sponsorship and support. Last but not least, we extend our thanks to the ETS'17 corporate sponsors: Advantest, ARM, Cadence, Intel, Mentor Graphics, NXP, Qualcomm, Qualtera, Ridgetop Europe, Synopsys, and Test Insight, for their financial sponsorship and continued support of ETS.

We are excited about the strong lineup of ETS'17 and overall of the European Test Week. We are confident that you will find it a beneficial and exciting experience with lots of networking opportunities for researchers, developers and vendors. We wish you all a fun-filled and productive week in Limassol!

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- H-M. VON STAUDT, DE
- X. WEN, JP

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- C. NICOPOULOS, CY
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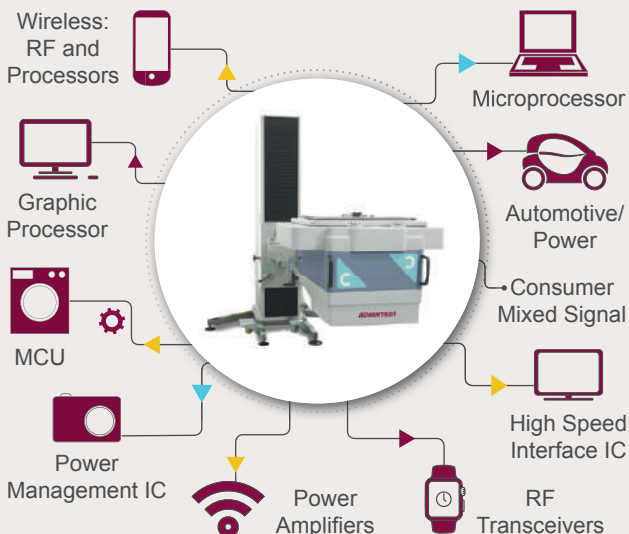
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## Organizers

University of Cyprus, CY.

KIOS Research and Innovation Center of Excellence, CY.

## Dates / Symposium Venue

<b>Dates</b>	May 22-26, 2017
<b>Venue</b>	AMATHUS BEACH HOTEL LIMASSOL 75 Amathounta Avenue 4532 Limassol, Cyprus P O Box 50513, 3606 Limassol, Cyprus
<b>Phone</b>	+357 2583 2000
<b>Fax</b>	+357 2583 2540
<b>Email</b>	amathusl@amathushotel.com
<b>Web</b>	<a href="http://www.amathuslimassol.com">http://www.amathuslimassol.com</a>

## Registration / Information Hours

<b>ETS/Workshops</b>	<b>Registration desk at Foyer</b>
Monday, May 22	12:00-18.30
Tuesday, May 23	08:00-19:30
Wednesday, May 24	08:00-15:00
Thursday, May 25	08:00-16:00

<b>Workshops Only</b>	<b>Registration desk at Foyer</b>
Thursday, May 25	16:00-20:00
Friday, May 26	08:00-16:30

## Board

The Welcome Reception will be held on Monday May 22, in the "Blue Breeze Lounge – Ground Floor". The Coffee breaks will be served in the "Atheneum Terrace". Lunches will be served in the "Kalypso Restaurant". The Social Event will take place at the *Kourion Archeological Site* followed by a gala dinner at the Evagoras Lanitis Centre - Carob Mill cultural center, which is situated in the Old Town of Limassol.

## Practical Information

### Travel Guide

Cyprus is easily accessible as it is linked with numerous direct and connecting flights with all the main European cities, Middle East, Africa and Asian countries. The legal ports of entry into the Republic of Cyprus are the airports of Larnaka (Larnaca) and Pafos (Paphos) and the ports of Larnaka (Larnaca), Lemesos (Limassol), Latsi and Pafos (Paphos), which are situated in the area under the effective control of the Government of the Republic of Cyprus.

Limassol is the island's second largest city. It spreads out between two ancient city-kingdoms, Amathous to the east and Kourion to the west, two of the most spectacular archaeological sites in Cyprus. It is the island's main port, the centre of the wine industry and a bustling holiday resort. A large number of hotels and hotel apartments line a 15 km coastline interspersed with eucalyptus groves and linked by a promenade popular with walkers or joggers.

### Public Transportation

For comprehensive information about public transportation in Cyprus, please visit the website <http://www.cyprusbybus.com>.

### Climate

Cyprus enjoys a Mediterranean climate with long dry summers from mid-May to mid-October and with mild winters from December to February, which are separated by short autumn and spring seasons. See <http://www.cyprus-weather.com> for more details.

### Language

Greek and Turkish are the official languages. English is widely spoken. French and German are also spoken within the tourism industry.

### Currency / Banking Hours / Credit Cards

The currency of the Republic of Cyprus is the Euro (€). Banking hours for the public: Monday-Friday 08:00 - 13:30. There

are many Automated Teller Machines (ATMs) outside most branches of banks in all towns and in the main tourist resorts. Hotels, large shops and restaurants normally accept credit cards and traveler's cheques. Banknotes of major foreign currencies are also acceptable. Rates of exchange are published daily in the local press and are broadcasted via the media.

### **Tipping**

Because of the 10% service charge levied in hotels and restaurants, a tip is not obligatory, but small change is always welcome. Taxi-drivers, porters, hairdressers etc., always appreciate a small tip.

### **Insurance**

It is recommended that participants arrange insurance for medical expenses, loss and accidents occurring during the conference. The organizers cannot be held responsible for any losses, damages or injuries.

### **Electric Current - Voltage**

The supply in Cyprus is 240 volts, a.c. 50Hz. Sockets are usually 13 amp, square pin in most buildings. Many hotels provide adaptors upon request from the reception.

### **General Shopping Hours**

Shop opening times vary depending on their type and location, though shops normally open between 07:00 and 09:00. During the period November 1st - March 31st shops close at 19:30 on Monday, Tuesday, Thursday and Friday, at 15:00 on Wednesday, and at 19:00 on Saturday. For the period April 1st - October 31st shops close at 20:00 on Monday, Tuesday, Thursday and Friday, at 15:00 on Wednesday and, at 19:30 on Saturday.

### **Chemist Pharmacies / Drug Stores**

They stay open during shopping hours. Late night chemists are listed in the daily papers.

# Main Conference Centre Mezzanine Floor

Aphrodite - 1

Poseidon - 2

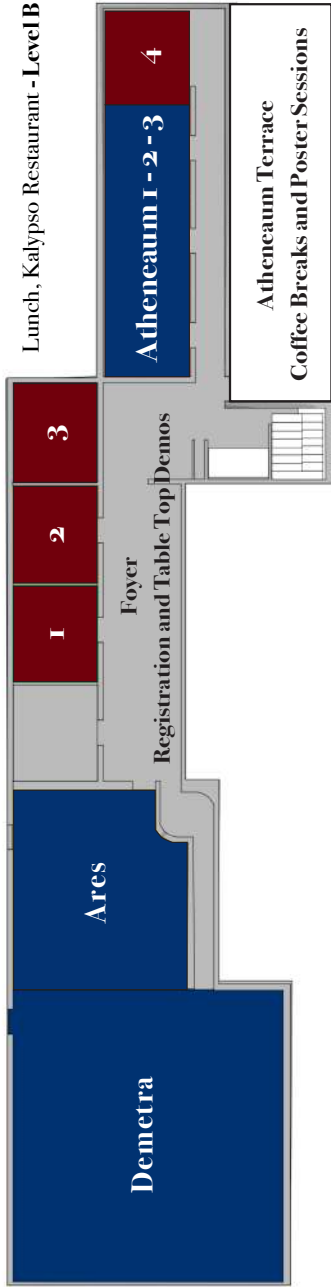
Business Centre - 3

Atheneum 4 - 4

Welcome Reception, Blue Breeze Bar - **Ground Floor**

Hera - **Ground Floor**

Lunch, Kalypso Restaurant - **Level B**



**14:00-18:30 TSS@ETS Tutorials**

*The TSS@ETS tutorials are accessible to all ETS attendees with a full registration.*

**14:00-16:00 Tutorial 1 (PART I) (Atheneum 1-3)**

**Moderator:** Lorena ANGHEL (TIMA, FR).

**Machine Learning Techniques for System Level Test and Diagnosis**

Krishnendu CHAKRABARTY (Duke Univ., US).

**14:00-16:00 Tutorial 2 (PART I) (Ares)**

**Moderator:** Hans-Joachim WUNDERLICH (Univ. of Stuttgart, DE).

**Self-Awareness and Resilience Against Faults, Bugs and Attacks**

Axel JANTSCH, Christian KRIEG (TU Wien, AT).

**16:00-16:30 Coffee Break (Atheneum Terrace)**

**16:30-18:30 Tutorial 1 (PART II) (Atheneum 1-3)**

**Moderator:** Lorena ANGHEL (TIMA, FR).

**Machine Learning Techniques for System Level Test and Diagnosis**

Krishnendu CHAKRABARTY (Duke Univ., US).

**16:30-18:30 Tutorial 2 (PART II) (Ares)**

**Moderator:** Hans-Joachim WUNDERLICH (Univ. of Stuttgart, DE).

**Self-Awareness and Resilience Against Faults, Bugs and Attacks**

Axel JANTSCH, Christian KRIEG (TU Wien, AT).

**18:30 - 19:00 Break**

**19:00 - 20:30 Welcome Reception  
(Blue Breeze Lounge – Ground Floor)**

## 8:30-09:00 Opening Session

(Demetra)

### Welcome Message

Maria K. MICHAEL (Univ. of Cyprus, KIOS, CY – ETS'17 General Chair).

### Welcome Message

Constantinos CHRISTOFIDES (Univ. of Cyprus, CY – Rector).

### Program Introduction

Haralampos-G. STRATIGOPOULOS (Sorbonne Univ., UPMC Univ. Paris 6, CNRS, LIP6, FR – ETS'17 Program Chair).

### Symposium Information

Stelios NEOPHYTOU (Univ. of Nicosia, CY – ETS'17 Local Arrangements Chair).

### ETS'16 Best Paper Award

Adit SINGH (Auburn Univ., US), Bernd BECKER (Univ. of Freiburg, DE) (ETS'16 Award Chairs).

### Test Technology Technical Council (TTTC) Awards

Yervant ZORIAN (Synopsys, US – TTTC President of Board).

## 9:00-10:00 Keynote Talk 1

(Demetra)

**Moderator:** Krishnendu CHAKRABARTY (Duke Univ., US).

**Smart Medical Devices for the Discovery and Treatment of Neurodegenerative Diseases** Mohamed SAWAN (Polytechnique Montréal, CA).

Dr. Sawan is a holder of a Canada Research Chair in Smart Medical Devices, is leading the Microsystems Strategic Alliance of Quebec (ReSMiQ), and is the founder of the Polystim Neurotechnologies Laboratory. This talk will cover circuit techniques and Microsystems intended to build various bioelectronic interfaces for intracortical neurorecording and microstimulation.

## 10:00-11:00 Coffee Break + Poster Session P1 + Table Top Demos

### 10:00-11:00 Table-Top Demos

(Foyer)

**Moderator:** Theocharis THEOCHARIDES (Univ. of Cyprus, KIOS, CY).

**D1. Silicon Debug, Characterization and Diagnosis Using Benchtop System** Wu YANG, Geir EIDE, Givargis DANIALY (Mentor Graphics, US).



TUESDAY, MAY 23, 2017

**D2. The SEcube™ Open Source Platform: Demo & Academy Program** Giuseppe AIRO FARULLA, Paolo PRINETTO (Politecnico di Torino, IT), Antonio VARRIALE (Blu5 Labs Ltd., MT).

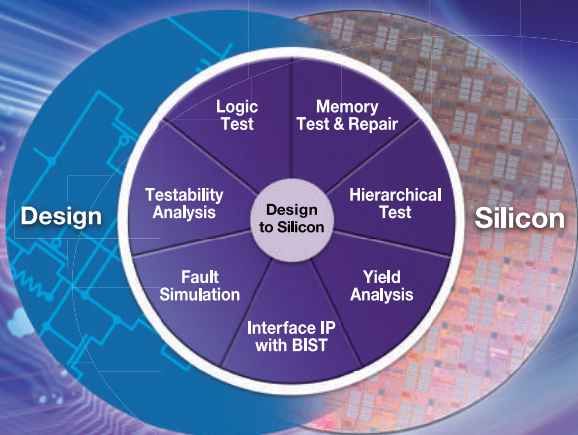
**D3. Qubit Test Synthesis for the Black Box Functionality** Vladimir HAHANOV, Eugenia LITVINOVA, Igor IEMELIANOV, Svetlana CHUMACHENKO, Hanna KHAKHANOVA (Kharkov National Univ. of Radioelectronics, UA), Wajeb GHARIBI (Jazan Univ., SA).

**D4. Quality and Reliability Test and Measurement Solutions** Hans MANHAEVE (Ridgetop Europe, BE).

**D5. CloudTesting Services for on Demand Silicon Validation and Verification** Stefan DOELLINGER (Advantest, DE).

**D6. Solving Congestion & Coverage Challenges In Next Generation Designs - Modus 2D Elastic Compression** Vladimir ZIVKOVIC (Cadence, UK).

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## 10:00-11:00 Poster Session P1 (Atheneum Terrace)

**Moderator:** Stelios NEOPHYTOU (Univ. of Nicosia, CY).

**P1.1 Detection of Resistive Open and Short Defects in FDSOI Under Delay-based Test: Optimal VDD and Body Biasing Conditions** Amit KAREL, Florence AZAIS, Mariane COMTE, Michel RENOVELL (Univ. of Montpellier II, CNRS, LIRMM, FR), Keshav SINGH (City Univ. of Hong Kong, HK), Zhang JING (Lund Univ., SE).

**P1.2 Mitigating Read & Write Errors in STT-MRAM Memories under DVS** Ioana VATAJELU (Univ. Grenoble Alpes, CNRS, TIMA, FR), Rosa RODRIGUEZ-MONTANES (Univ. Politècnica de Catalunya, ES), Michel RENOVELL (Univ. of Montpellier II, CNRS, LIRMM, FR), Joan FIGUERAS (Univ. Politècnica de Catalunya, ES).

**P1.3 Extension of Power Supply Impedance Emulation Method on ATE for Multiple Power Domain** Naoki TERAO, Toru NAKURA (Univ. of Tokyo, JP), Masahiro ISHIDA (Advantest, JP), Rimon IKENO (Univ. of Tokyo, JP), Takashi KUSAKA (Advantest, JP), Tetsuya IZUKA, Kunihiro ASADA (Univ. of Tokyo, JP).

**P1.4 Automated Area and Coverage Optimization of Minimal Latency Checkers** Siavoosh PAYANDEH AZAD, Behrad NIAZMAND, Apneet KAUR SANDHU, Jaan RAIK, Gert JERVAN, Thomas HOLLSTEIN (Tallinn Univ. of Technology, EE).

**P1.5 A Homogeneous Framework for AMS Languages Instrumentation, Abstraction and Simulation** Enrico FRACCAROLI, Luca PICCOLBONI, Franco FUMMI (Univ. of Verona, IT).

**P1.6 Integrated Circuits' Characterization for Non-normal Data in Semiconductor Quality Analysis** Ingrid KOVACS (Technical Univ. of Cluj-Napoca, RO), Andi BUZO, Georg PELZ (Infineon Technologies, DE), Marina TOPA (Technical Univ. of Cluj-Napoca, RO).

11:00-12:30 **1A. Regular Session 1** (Demetra)

## **Analog, Mixed-Signal, RF, and MEMS I**

**Moderators:** Alkis HATZOPOULOS (Aristotle Univ. of Thessaloniki, GR), Gildas LEGER (Instituto de Microelectrónica de Sevilla, ES).

**Design of a Sinusoidal Signal Generator with Calibrated Harmonic Cancellation for Mixed-signal BIST in a 28 nm FDSOI Technology** Hani MALLOUG, Manuel BARRAGAN, Salvador MIR (Univ. Grenoble Alpes, CNRS, TIMA, FR), Laurent BASTERES, Herve LE GALL (STMicroelectronics, FR).

**Automatic Testing of Analog ICs for Latent Defects using Topology Modification** Nektar XAMA, Anthony COYETTE, Baris ESEN (KU Leuven, BE), Wim DOBBELAERE, Ronny VANHOOREN (ON Semiconductor, BE), Georges GIELEN (KU Leuven, BE).

**Contact-less Near-Field Measurement of RF Phased Array Mismatches** Maryam SHAFIEE, Sule OZEV (Arizona State Univ., US).

11:00-12:30 **1B. ETS<sup>2</sup> Session 1** (Ares)

## **On Launching an Automotive Product with an Immediate Guaranteed High Quality and Yield**

**Moderators:** Rene SEGERS (ReSeCo, NL), Bernd BECKER (Univ. of Freiburg, DE).

**Designing for Automotive Quality: Practical DFM and DFT Considerations** Thomas HERMANN (GLOBAL-FOUNDRIES, DE).

**First Time Right Test Set-Up: Key for a Perfect Automotive Launch** Robert VAN RIJSINGE (NXP, NL).

**Experience and Expectations of Automotive Suppliers for Smooth Launch** Viktor MUELLER (Continental, DE).

11:00-12:30 **1C. Vendor Session 1**  
(Atheneum 1-3)

**Moderators:** Ashraf SALEM (Mentor Graphics, EG), Paul-Henri PUGLIESI-CONTI (NXP, FR).

TUESDAY, MAY 23, 2017

**Faster and Fewer Patterns with Breakthrough ATPG to the Rescue** Rohit KAPUR (Synopsys, US).

**The DFT Challenges and Solutions for the ARM® Mali™-Mimir GPU** Teresa MCLAURIN (ARM, US), Prashant KULKARNI (ARM, UK).

**Full Throttle on Automotive Test** Martin KEIM, Stephen PATERAS, Becki WATT (Mentor Graphics, US).

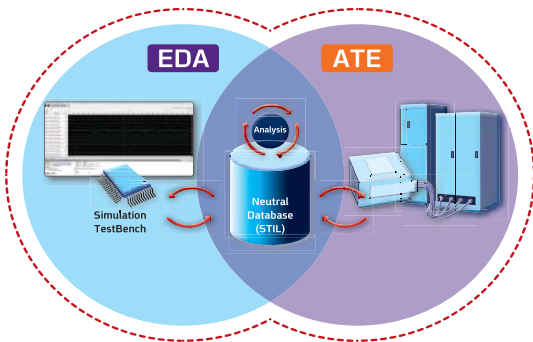
12:30-14:00 **Lunch**

(Kalypso Restaurant)

tesT insight

## Tester Data Link

High-performance conversion between EDA and ATE



Semiconductor test engineers face two main challenges when performing a definitive final test. They must verify that no information is lost during the conversion between the design and testing phases, and produce a final test that is fully aligned with the design goals. Partial or inaccurate test results present a serious quality risk, resulting in device failure, decreased yield, or defective device approval. A closed loop between the design stage and the test environment is essential for final test integrity.

Test Insight's **Tester Data Link (TDL)** customizes test patterns that were created using the EDA simulation environment in order to match the unique characteristics of the ATE. Comprising three primary modules - VCD2STIL, ATEGen and VT - the solution creates a definitive link between the design and test phases, increasing productivity and reducing costs. TDL enables advanced program debugging - even before the silicon arrives.

14:00-15:30 **2A. Special Session 1** (Demetra)

## **Design and Test Needs for Adaptive, Self-Learning and Cognitive Systems**

**Moderator:** Shreyas SEN (Purdue Univ., US).

**Energy-efficient Cognitive Computing** Kaushik ROY (Purdue Univ., US).

**Design and Test Needs for Adaptive IoT Sensor Nodes** Shreyas SEN (Purdue Univ., US), Arijit RAYCHOWDHURY (Georgia Inst. of Technology, US).

**Self-Learning Systems: Opportunities and Challenges** Abhijit CHATTERJEE (Georgia Inst. of Technology, US).

14:00-15:30 **2B. ETS<sup>2</sup> Session 2** (Ares)

## **How to Get the Required Quality and Reliability at Reasonable (Test) Costs?**

**Moderators:** Rene SEGERS (ReSeCo, NL), Bernd BECKER (Univ. of Freiburg, DE).

**Limitation of Scan Diagnosis Leading to New Tools Required for Debugging Scan Problems** Ralf ARNOLD (Infineon, DE).

**On Emerging Packaging Defects Impacting Reliability and Test Coverage** Davide APPELLO (STMicroelectronics, IT).

**How do we Manage the Profusion of New Tests Being Generated to Improve Quality?** Peter MAXWELL (ON Semiconductor, US).

14:00-15:30 **2C. Vendor Session 2**  
(Atheneum 1-3)

**Moderators:** Juergen SCHLOEFFEL (Mentor Graphics, DE), Michele PORTOLAN (Univ. Grenoble Alpes, CNRS, TIMA, FR).

**Functional Safety Support for IP - or What Exactly is an SEooC?** Pete HARROD (ARM, UK).

**DFT Methodologies and IoT Trend** Kan THAPAR (Mentor Graphics, UK), Becki WATT (Mentor Graphics, US).

**Reliability - A Nanometer Nightmare?** Hans MANHAEVE (Ridgetop Europe, BE).

15:30-16:00 **Coffee Break** (Atheneum Terrace)

16:00-17:30 **3A. Regular Session 2** (Demetra)

### **Self-learning, Adaptation, Fault Tolerance, Approximate Computing**

**Moderators:** Chrysostomos NICOPOULOS (Univ. of Cyprus, CY), Michel RENOVELL (Univ. of Montpellier II, CNRS, LIRMM, FR).

#### **Exploiting STT-MRAM for Approximate Computing**

Nour SAYED, Fabian OBORIL, Azadeh SHIRVANIAN, Rajendra BISHNOI, Mehdi TAHOORI (Karlsruhe Institute of Technology, DE).

#### **Real-Time Self-Learning For Control Law Adaptation In Nonlinear Systems Using Encoded Check State**

Suvadeep BANERJEE, Abhijit CHATTERJEE (Georgia Institute of Technology, US).

#### **Rout3D: A Lightweight Adaptive Routing Algorithm for Tolerating Faulty Vertical Links in 3D-NoCs**

Zergainoh NACER-EDDINE, Amir CHARIF, Alexandre COELHO, Michael NICOLAIDIS (Univ. Grenoble Alpes, CNRS, TIMA, FR).

16:00-17:30 **3B. ETS<sup>2</sup> Session 3** (Ares)

### **How Does the AMS Area Cope with the High Quality Requirements?**

**Moderators:** Rene SEGERS (ReSeCo, NL), Bernd BECKER (Univ. of Freiburg, DE).

#### **Testing of Mixed Signal Automotive Circuits: Do We Guarantee the Spec or Do We Catch Defects?**

Wim DOBBELAERE (ON Semiconductor, BE).

#### **Who Solves the Mixed-Signal DfT Challenges?**

Hans-Martin VON STAUDT (Dialog Semiconductor, DE).

#### **A Publicly-Accessible Set of AMS Benchmark Circuits**

Stephen SUNTER (Mentor Graphics, CA).

16:00-17:30 **3C. Vendor Session 3**

(Atheneum 1-3)

**Moderators:** Stefano DI CARLO (Politecnico di Torino, IT), Erik LARSSON (Lund Univ., SE).

**Dependability & Test for Safety Critical Applications**

Vladimir ZIVKOVIC (Cadence, UK).

**Bringing Embedded Instruments from Laboratory to Production Test**

Artur JUTMAN, Sergei ODINTSOV, Sergei DEVADZE, Igor ALEKSEJEV (Testonica Lab OÜ, EE).

**An End-to-end Test & Repair Solution**

Yervant ZORIAN (Synopsys, US), Gurgun HARUTYUNYAN (Synopsys, AM).

17:30-18:00 **Break**

18:00-19:30 **4A. Wine & Cheese Panel 1 (Demetra)**

**What are the Most Significant Defects that we are not Modeling or Targeting Adequately?**

**Moderator:** Stephen SUNTER (Mentor Graphics, CA).

**Panelists:** Davide APPELLO (STMicroelectronics, IT), John CARULLI (GLOBALFOUNDRIES, US), Wim DOBBELAERE (ON Semiconductor, BE), Adit SINGH (Auburn Univ., US), Vladimir ZIVKOVIC (Cadence, UK).

18:00-19:30 **4B. Wine & Cheese Panel 2 (Ares)**

**In-field Self-test for Automotive ICs: which Solutions are Going to Prevail and why?**

**Moderator:** Matteo SONZA REORDA (Politecnico di Torino, IT).

**Panelists:** Teresa MCLAURIN (ARM, US), Martin KEIM (Mentor Graphics, US), Ernesto SANCHEZ (Politecnico di Torino, IT), Yervant ZORIAN (Synopsys, US).

# 22<sup>nd</sup> IEEE European Test Symposium 2017 – Program at a Glance

Day	MONDAY - May 22	TUESDAY - May 23	WEDNESDAY - May 24	THURSDAY - May 25	FRIDAY - May 26
Room	Atheneum 1-3	Ares	Atheneum 1-3	Ares	Atheneum 1-3
08:00-08:30	Registration @Foyer				
08:30-09:00	Registration @Foyer				
09:00-09:30	<b>Plenary Keynote 2:</b> Hans-Juergen Wagner, Advantest Europe GmbH @Demetra				
09:30-10:00	<b>Plenary Keynote 1:</b> Mohamad Sawan, Polytechnique Montreal, Canada @Demetra				
10:00-10:30	Coffee Break + Poster Session 1 + Table-Top Demos @Atheneum Terrace & Foyer				
10:30-11:00	Coffee Break + Poster Session 2 + Table-Top Demos @Atheneum Terrace & Foyer				
11:00-11:30	Regular Session 1: AMS, RF & MEMS I	ETS <sup>2</sup> 1: Launching automotive chips with high quality and yield	Regular Session 3: Digital Test	Regular Session 8: Security	Coffee Break @Atheneum Terrace + Poster Session
11:30-12:00	Special Session 1: Adaptive, Self-Learning	Vendor Session 1	Regular Session 4: Memories I	Regular Session 2: Testing for Automobile	RESOLVE Workshop
12:00-12:30	TSS@ETS Tutorial 1: Self-Awareness	ETS <sup>2</sup> 2: Quality and Reliability at the Edge	Regular Session 5: Diagnosis II	Special Session 3: Big Data for Test Engineering	TESTA Workshop
12:30-13:00	Registration @Foyer	Lunch Break @Kalypso Restaurant			Lunch Break @Kalypso Restaurant
13:00-13:30	TSS@ETS Tutorial 2: Self-Awareness	Vendor Session 2	Regular Session 6: Memories II	Special Session 8: Security	RESOLVE Workshop
13:30-14:00	TSS@ETS Tutorial 1: Self-Awareness	ETS <sup>2</sup> 3: Quality and Reliability at the Edge	Regular Session 7: AMS, RF & MEMS II	McCluskey PHD Thesis Award	TESTA Workshop
14:00-14:30	TSS@ETS Tutorial 2: Self-Awareness	ETS <sup>2</sup> 4: Quality and Reliability at the Edge	Embedded Tutorial 3: Volume Diagnosis in 2.5D and 3D Systems	Embedded Tutorial 1: Countering Malicious Faults in Crypto Circuits	RESOLVE Workshop
14:30-15:00	TSS@ETS Tutorial 1: Self-Awareness	ETS <sup>2</sup> 5: Quality and Reliability at the Edge	Embedded Tutorial 4: Testing IO interfaces in 2.5D and 3D Systems	Embedded Tutorial 2: Security and Trust for AMS/RF Domain	TESTA Workshop
				Industry Wish List @Demetra	



15:00-15:30	Machine Learning for System Level Test and Diagnosis	Learning, Cognitive Systems	Reasonable (test) costs	Break
15:30-16:00	Machine Learning and Resilience Against Faults, Bugs and Attacks			
16:00-16:30	Coffee Break @Athenaeum Terrace	Coffee Break @Athenaeum Terrace		
16:30-17:00	TSS@ETS Tutorial 1: Machine Learning and Resilience Against Faults, Bugs and Attacks	Regular Session 2: Fault Tolerance and Approximate Computing	ETS <sup>2</sup> 3: AMS vs. high quality requirements	Vendor Session 3
17:00-17:30	TSS@ETS Tutorial 2: Self-Awareness and Resilience Against Faults, Bugs and Attacks			
17:30-18:00	Machine Learning for System Level Test and Diagnosis			
18:00-18:30	Break	Wine & Cheese Panel 1: What are the most significant defects not modeled or targeted adequately?	Wine & Cheese Panel 2: In-field self-test for automotive ICs: which solutions?	Break
18:30-19:00	Break			
19:00-19:30	Break			
19:30-20:00	Welcome Reception @Blue Breeze Lounge			
20:00-20:30				
20:30-21:00				
21:00-21:30				
Social Event (15:30 - 22:30)				
Colloquium in Honor of Joan Figueras				
		RESQUC Workshop	TESTA Workshop	RESQUC Workshop
		Workshop Registration / Coffee Break @Foyer / @Athenaeum Terrace		
		Conference Closing @Demetra		
		Coffee Break @Athenaeum Terrace		
		TESTA Workshop		
		Workshops' Joint Welcome Reception @Blue Breeze Lounge		
		TESTA & RESQUC Workshops Joint Panel @Ares		
		Break		

### Fringe Meetings

	Date and Time	Location
ETS Steering Committee Meeting	Mon. May 22, 16:00–19:00	Hera
ETM – European Test Meeting	Mon. May 22, 14:00–19:00	Poseidon
ETS Steering Committee Meeting	Tue. May 23, 12:30–14:00	Hera
ETTTC Meeting	Wed. May 24, 12:30–14:00	Hera
ETS'18 Executive Committee Meeting	Thu. May 25, 12:30–14:00	Hera
H2020 RESQUC Project Management Committee Meeting	Fri. May 26, 16:45–20:00	Ares

08:30-09:30 **Keynote Talk 2** (Demetra)

**Moderator:** Jochen RIVOIR (Advantest, DE).

**The Future Trends and Contributions of Test in the SOC Market** Hans-Juergen WAGNER (Advantest, DE).

Hans-Juergen is Managing Director at Advantest Europe GmbH and also a Managing Executive Officer at Advantest Corporation. He currently leads the System-on-a-Chip Test Business Group and is a valued member of the Senior Executive Staff. In this keynote he will talk about the new mega-trends, such as IoT, Industry4.0, ADAS, 5G, and Big Data, their requirements and highlight how ATE-based solutions can or must contribute to these trends.

9:30-10:30 **Coffee Break + Poster Session P2**  
+ **Table Top Demos**

9:30-10:30 **Table-Top Demos** (Foyer)

**Moderator:** Theocharis THEOCHARIDES (Univ. of Cyprus, KIOS, CY).

*For the complete list of Table-Top Demos, see program on Tuesday, May 23, 2017, 10:00-11:00.*

9:30-10:30 **Poster Session P2** (Atheneum Terrace)

**Moderator:** Stelios NEOPHYTOU (Univ. of Nicosia, CY).

**P2.1 ISO26262-Compliant Soft Error Mitigation in Memory Banks** Jan SCHAT (NXP, DE).

**P2.2 Periodic Bias-Temperature Instability Monitoring in SRAM Cells** Yiorgos TSIATOUHAS (Univ. of Ioannina, GR).

**P2.3 Mixed-Signal BIST Computation Offloading Using IEEE 1687** Michele PORTOLAN, Manuel BARRAGAN, Rshdee ALHAKIM, Salvador MIR (Univ. Grenoble Alpes, CNRS, TIMA, FR).

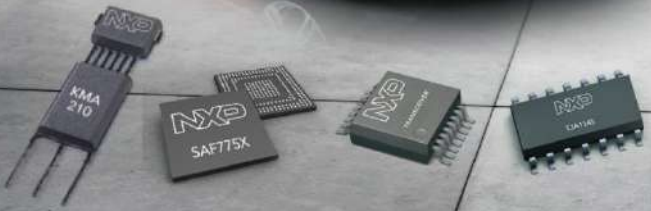
**P2.4 Impact of the Switching Activity on the Aging of Delay PUFs** Naghmeh KARIMI (Univ. of Maryland Baltimore County, US), Jean-Luc DANGER, Mariem SLIMANI, Sylvain GUILLEY (Telecom ParisTech, Univ. Paris-Saclay, FR).

WEDNESDAY, MAY 24, 2017

**P2.5 Derivation of the Reliability Metric for Digital Circuits** Mohamed ABUFALGHA, Alex BYSTROV (Newcastle Univ., UK).

**P2.6 A Very Low Cost and Highly Parallel DFT Method for Analog and Mixed-Signal Circuits** Baris ESEN, Anthony COYETTE, Nektar XAMA (KU Leuven, Belgium), Wim DOBBELAERE, Ronny VANHOOREN (ON Semiconductor, BE), Georges GIELEN (KU Leuven, Belgium).

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10:30-11:30 **5A. Regular Session 3** (Demetra)

**Digital Test**

**Moderators:** Grzegorz MRUGALSKI (Mentor Graphics, PL), Stephan EGGERSGLÜSS (Univ. of Bremen, DE).

**Probabilistic Sensitization Analysis for Variation-Aware Path Delay Fault Test Evaluation** Marcus WAGNER, Hans-Joachim WUNDERLICH (Univ. of Stuttgart, DE).

**Bridge Over Troubled Waters: Critical Area Based Pattern Generation** Peter MAXWELL (ON Semiconductor, US), Friedrich HAPKE, Maija RYYNANEN, Peter WESELOH (Mentor Graphics, DE).

10:30-11:30 **5B. Regular Session 4** (Ares)

**Memories I**

**Moderators:** Elena Ioana VATAJELU (Univ. Grenoble Alpes, CNRS, TIMA, FR), Yiorgos TSIATOUHAS (Univ. of Ioannina, GR).

**Aging-Aware Coding Scheme for Memory Arrays** Mohammad Saber GOLANBARI, Nour SAYED, Mojtaba EBRAHIMI, Mohammad Hadi MOSHREFPOUR ESFAHANY, Saman KIAMEHR, Mehdi TAHOORI (Karlsruhe Institute of Technology, DE).

**ROM Fault Diagnosis for  $O(n^2)$  Test Algorithms** Artur POGIEL (Mentor Graphics, PL), Janusz RAJSKI (Mentor Graphics, US), Jerzy TYSZER (Poznan Univ. of Technology, PL).

10:30-11:30 **5C. Embedded Tutorial 1**  
(Atheneum 1-3)

**Moderator:** Alex ORAILOGLU (Univ. of California, San Diego, US).

**Counteracting Malicious Faults in Cryptographic Circuits** Iliia POLIAN (Univ. of Passau, DE), Francesco REGAZZONI (ALaRI Institute, Univ. of Lugano, CH).

10:30-12:30 TTTC's E. J. McCluskey Doctoral Thesis Award – ETS Semi-Finals (Atheneum 4)

11:30-12:30 6A. Regular Session 5 (Demetra)  
**Diagnosis and Failure Analysis**

**Moderators:** Alberto BOSIO (Univ. of Montpellier II, CNRS, LIRMM, FR), Michiko INOUE (Nara Institute of Science and Technology, JP).

**Multiple-Defect Diagnosis for Logic Characterization Vehicles** Benjamin NIEWENHUIS, Soumya MITTAL, Ronald BLANTON (Carnegie Mellon Univ., US).

**Data-driven Fault Diagnosis with Missing Syndromes Imputation for Functional Test through Conditional Specification** Tong GUAN (State Univ. of New York at Buffalo,US), Zhaobo ZHANG (Huawei Technologies, US), Wen DONG, Chunming QIAO (State Univ. of New York at Buffalo,US), Xinli Gu (Huawei Technologies, US).



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11:30-12:30 **6B. Regular Session 6** (Ares)

## Memories II

**Moderators:** Liviu MICLEA (Technical Univ. of Cluj-Napoca, RO), Sybille HELLEBRAND (Univ. of Paderborn, DE).

**Refresh Frequency Reduction of Data Stored in SSDs Based on A-timer and Timestamps** Marcelino SEIF, Emna FARJALLAH, Franck BADETS, Christophe LAYER, Emna CHABCHOUB, Jean-marc ARMANI, Francis JOFFRE (CEA LIST, FR), Costin ANGHEL (Institut Supérieur d'Electronique de Paris, FR), Luigi DILILLO (Univ. of Montpellier II, CNRS, LIRMM, FR), Valentin GHERMAN (CEA LIST, FR).

**Online Profiling for Cluster-Specific Variable Rate Refreshing in High-Density DRAM Systems** Rasool SHARIFI, Zainalabedin NAVABI (Univ. of Tehran, IR).

11:30-12:30 **6C. Embedded Tutorial 2**  
(Atheneum 1-3)

**Moderator:** Giorgio DI NATALE (Univ. of Montpellier II, CNRS, LIRMM, FR).

**Security and Trust in the Analog/Mixed-Signal/RF Domain: A Survey and a Perspective** Yiorgos MAKRIS (UT Dallas, US).

12:30-14:00 **Lunch** (Kalypso Restaurant)

14:00-15:00 **7A. Regular Session 7** (Demetra)

## Analog, Mixed-Signal, RF and MEMS II

**Moderators:** Marie-Minerve LOUËRAT (Sorbonne Univ., UPMC Univ. Paris 6, CNRS, LIP6, FR), Hans KERKHOFF (Univ. of Twente, NL).

**A Phase Locking Test Solution for MEMS Devices** Tareq SUPON, Rashid RASHIDZADEH (Univ. of Windsor, CA).

**Coverage-driven Mixed-signal Verification of Smart Power ICs in a UVM Environment** Sebastian SIMON, Deeksha BHAT, Alexander RATH, Jérôme KIRSCHER, Sebastian SIMON (Infineon Technologies AG, DE), Linus MAURER (Bundeswehr Univ. Munich, DE).

14:00-15:00 **7B. Embedded Tutorial 3** (Ares)

**Moderator:** Paolo BERNARDI (Politecnico di Torino, IT).

**Volume Diagnosis Data Mining** Wu-Tung CHENG (Mentor Graphics, US), Yue TIAN, Sudhakar M. REDDY (Univ. of Iowa, US).


14:00-15:00 **7C. Embedded Tutorial 4**  
(Atheneum 1-3)

**Moderator:** David KEEZER (Georgia Institute of Technology, US).

**Challenges and Emerging Solutions in Testing Embedded IO interfaces in 2.5D and 3D Systems**  
Salem ABDENNADHER (Intel, US).

15:00-15:30 **Break**

15:30-22:30 **Social Event & Dinner**

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09:00-10:00 **Keynote Talk 3** (Demetra)

**Moderator:** Rob AITKEN (ARM, US).

**To a Trillion and Beyond, the Future of the Internet of Things** Krisztián FLAUTNER (ARM, US).

Krisztián Flautner is the vice president of technology for Incubation Businesses at ARM. He is focused on new business opportunities and the proliferation of ARM technologies, including creating a platform and ecosystem that accelerates time to market for secure, managed, connected products. In this keynote he will talk about the need for renewed concentration on automatable and provable approaches to resilience, security, test and verification. He will also discuss challenges on how to measure trust and design it into systems, how to test whether AI is working correctly, and how to ensure the legitimacy of the data underpinning it all.

10:00-11:00 **Coffee Break + Poster Session P3 + Table Top Demos**

10:00-11:00 **Table-Top Demos** (Foyer)

**Moderator:** Theocharis THEOCHARIDES (Univ. of Cyprus, KIOS Research and Innovation Center of Excellence, CY).

*For the complete list of Table-Top Demos, see program on Tuesday, May 23, 2017, 10:00-11:00.*

10:00-11:00 **Poster Session P3** (Atheneum Terrace)

**Moderator:** Stelios NEOPHYTOU (Univ. of Nicosia, CY).

**P3.1 Low Power Probabilistic Online Monitoring of Systematic Erroneous Behaviour** Mauricio GUTIERREZ, Vasileios TENENTES (Univ. of Southampton, UK), Daniele Rossi (Univ. of Westminster, UK), Tom KAZMIERSKI (Univ. of Southampton, UK).

**P3.2 SIC Pair Generation in Optimal Time using Rotatable Counters** Ioannis VOYIATZIS (TEI of Athens, GR).

**P3.3 An Efficient Test Technique to Prevent Scan-Based Side-Channel Attacks** Satyadev AHLAWAT, Darshit VAGHANI, Virendra SINGH (Indian Institute of Technology Bombay, IN).



**P3.4 Application-Aware Lifetime Estimation of Power Devices** Ciprian POP (Univ. Politehnica of Bucharest, RO and Infineon Technologies, DE), Corneliu BURILEANU (Univ. Politehnica of Bucharest, RO), Andi BUZO, Georg PELZ (Infineon Technologies, DE).

**P3.5 Improving the Dependability of AMR Sensors used in Automotive Applications** Andreina ZAMBRANO, Hans KERKHOFF (Univ. of Twente, NL).

**P3.6 Extended Binary Nonlinear Codes and Their Application in Testing and Compression** Ondrej NOVAK (TU of Liberec, CZ).

**P3.7 A Built-In Self-Test Scheme for Classifying Refresh Periods of DRAMs** Chia-Ming CHANG, Yong-Xiao CHEN, Jin-Fu LI (National Central Univ., TW).

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11:00-12:30 **8A. Regular Session 8** (Demetra)  
**Security**

**Moderators:** Michael MANIATAKOS (NYU Abu Dhabi, AE), Iliia POLIAN (Univ. of Passau, DE).

**Detecting Hardware Trojans Without A Golden IC Through Clock-Tree Defined Circuit Partitions** Fakir HOSSAIN, Tomokazu YONEDA, Michiko INOUE (Nara Institute of Science and Technology, JP), Alex ORAILOGLU (UC San Diego, US).

**Specification and Verification of Security in Re-configurable Scan Networks** Michael KOCHTE (Univ. of Stuttgart, DE), Matthias SAUER (Univ. of Freiburg, DE), Laura RODRIGUEZ GOMEZ (Univ. of Stuttgart, DE), Pascal RAIOLA, Bernd BECKER (Univ. of Freiburg, DE), Hans-Joachim WUNDERLICH (Univ. of Stuttgart, DE).

**Scan Chain Encryption for the Test, Diagnosis and Debug of Secure Circuits** Mathieu DA SILVA, Marie-Lise FLOTTES (Univ. of Montpellier II, CNRS, LIRMM, FR), Giorgio DI NATALE, Bruno ROUZEYRE (Univ. of Montpellier II, CNRS, LIRMM, FR), Marco RESTIFO, Paolo PRINETTO (Politecnico di Torino, IT).

11:00-12:30 **8B. Special Session 2** (Ares)

**Testing for Automotive: What Are the Needs and What Are the Solutions?**

**Moderator:** Hans MANHAEVE (Ridgetop Europe, BE).

**ISO 26262 Fault Detection and Testing, What's Required?** Mathieu BLAZY-WINNING (NXP, FR).

**The Challenges of Test for Automotive Applications - An IP Provider's Perspective** Pete HARROD (ARM, UK).

**Automotive Expectation for Semiconductor Testability** Viktor MUELLER (Continental, DE).

**Functional Safety Requirements and Solutions for Automotive SoCs** Gurgen HARUTYUNYAN (Synopsys, AM).

11:00-12:30 **8C. Special Session 3**

**Big Data for Test Engineering:  
Opportunities and Challenges**

(Atheneum 1-3)

**Moderator:** Said HAMDIOUI (TU Delft, NL).

**Big Data Yield Learning Aspects** Thomas HERRMANN  
(GLOBALFOUNDRIES, DE).

**Using Big Data to Enable Part-level Prediction in the  
Supply Chain** Stéphane LUNG (Qualtera, FR).

**Big Data for Test Engineering** Keith ARNOLD (PDF  
Solutions, US).

12:30-14:00 **Lunch**

(Kalypso Restaurant)

14:00-15:30 **9. Industry Wish List**

(Demetra)

**Moderators:** Peter MAXWELL (ON Semiconductor, US),  
Sule OZEV (Arizona State Univ., US).

**Speakers:** John CARULLI (GLOBALFOUNDRIES, US), Xinli  
Gu (Huawei Technologies, US), Peter WOHL (Synopsys, US),  
Hans MANHAEVE (Ridgetop Europe, BE), Kan THAPAR (Mentor  
Graphics, UK), Yervant ZORIAN (Synopsys, US), Keith ARNOLD  
(PDF Solutions, US).

15:30-16:00 **Closing Session**

(Demetra)

**Closing Message**

Maria K. MICHAEL (Univ. of Cyprus, KIOS Research and  
Innovation Center of Excellence, CY – ETS'17 General Chair).

**ETS'18 Introduction**

Rolf DRECHSLER, Stephan EGGERSGLÜSS (Univ. of Bremen, DE  
– ETS'18 General Chairs).

Two workshops are co-located with ETS'17 in Limassol. Both of them will take place in parallel from Thursday, May 25, 16:00, till Friday, May 26, 16:30.

## 2<sup>nd</sup> International Test Standards Application Workshop (TESTA 2017)

### Scope and Mission

**General Chair:** Artur JUTMAN (Testonica Lab, EE)

**General Co-Chair:** Michele PORTOLAN (TIMA Laboratory, FR)

**Program Chairs:** Al CROUCH (SiliconAid, US), Rene KRENZ-BAATH (Hamm-Lippstadt University, DE)

**Brief Description:** TESTA workshop is a focused open discussion platform dedicated to exchange of fresh ideas, industrial best practices, methodologies and work-in-progress around test-related standards, especially those being actively developed today or the ones recently released. The organizing committee pursues contributions covering IEEE 1149.x, IEEE 1500, IEEE 1687, IEEE P1838, IEEE 1450, etc., especially those focusing on what works, what doesn't, or how the standards were incorporated into existing or new DFT methodologies. Reports on first-time usage of the new and upcoming standards are especially welcome, as is research exploring the best usage of features described in these standards.

For more information and the workshop program visit <http://www.iti.uni-stuttgart.de/testa2017/>.

## RESCUE: Workshop on Reliability, Security and Quality

**General Chair:**

Francesco REGAZZONI (University of Lugano, CH)

**General Co-Chair:**

Maksim JENIHHIN (Tallinn University of Technology, EE)

**Program Chair:**

Ofer HADAR (Ben Gurion University of the Negev, IL)

**Program Co-Chair:**

Matteo SONZA REORDA (Politecnico di Torino, IT)

**Brief Description:** Relationship between reliability, quality and security is contradictory: despite pursuing the same goal, i.e. the safe and correct operation of a computing system, they start from completely different assumptions. Quality and reliability address technical errors occurring during design and manufacturing of the computing system and along its lifetime, while security aims at defeating malicious attempts of altering the normal behavior of the system. These design aspects set mutual constraints and contradicting requirements, nevertheless techniques from one discipline can be successfully applied to the other (e.g., fault tolerance to counteract fault injection attacks). Eventually, designers should guarantee the correct operation of the system, regardless of origin of the malfunctioning, i.e. being it malicious or technical. In this context, it is essential that designers are aware of the complete picture, and that researchers from the these interdependent disciplines meet and exchange ideas and challenges. RESCUE workshop establishes an open forum to bringing together the security community with the reliability, testing/verification communities to encourage fruitful discussions and collaborations involving researchers from both academic and industrial sectors. The workshop targets at designers of hardware and software layers of computing systems. The attendees are expected from both the security community and from the reliability, testing/verification communities.

For more information and the workshop program visit <http://www.ets17.org.cy/workshop/rescue-workshop.html>.

# TESSENT<sup>®</sup>

## LEADING AUTOMOTIVE TEST AND DIAGNOSIS SOLUTIONS



**MENTOR GRAPHICS IS A PROUD SUPPORTER  
OF THE 2017 EUROPEAN TEST SYMPOSIUM**

Mentor Graphics Tessent product line covers everything from test definition, test bring-up, silicon characterization, water test, package test, failure diagnosis and yield analysis for IC logic, memory, analog, and I/O. Tessent includes a comprehensive set of targeted test solutions to meet ISO 26262 quality and reliability requirements. All Tessent solutions are part of the Mentor Safe program and are ISO 26262 certified for use on ASIL D designs. Visit our website at [go.mentor.com/sts](http://go.mentor.com/sts)

**Mentor  
Graphics<sup>®</sup>**

THE EDA TECHNOLOGY LEADER

### **ETS Steering Committee Meeting**

*Chair:* Matteo SONZA REORDA

Monday, May 22, from 16:00 to 19:00

Room "Hera"

### **ETM – European Test Meeting**

*Chair:* Rene SEGERS

Monday, May 22, from 14:00 to 19:00

Room "Poseidon"

### **ETS Steering Committee Meeting**

*Chair:* Matteo SONZA REORDA

Tuesday, May 23, from 12:30 to 14:00

Room "Hera"

### **ETTTC Meeting**

*Chair:* Giorgio DI NATALE

Wednesday, May 24, from 12:30 to 14:00

Room "Hera"

### **ETS18 Executive meeting**

*Chairs:* Rolf DRECHSLER, Stephan EGGERSGLÜSS, Bernd BECKER

Thursday May 25, from 12:30 to 14:00

Room "Hera"

### **H2020 RESCUE Project Management Committee Meeting**

*Chair:* Maksim JENIHHIN

Friday, May 26, from 16:45 to 20:00

Room "Ares"

# Qualtera

Enterprise big data solutions  
for test and manufacturing

## Welcome Reception

The Welcome Reception will take place on Monday, May 22, from 19:00 to 20:30 at Blue Breeze Lounge, Ground Floor of Amathus Beach Hotel. Drinks and small snacks will be served.

## Social Event

The Social Event on Wednesday, May 24, will take place at the Kourion Archeological Site followed by a gala dinner at the Evagoras Lanitis Centre - Carob Mill cultural center, which is situated in the old town of Limassol.

Busses will depart sharply on 15:30 from the Conference Venue. Comfortable clothing and shoes are recommended.

### 15:30-19:30 – Kourion Archaeological Site

Driving through the vineyards and citrus plantations of Fasouri we will visit the ancient city of Kourion, an impressive Greco-Roman unspoiled site which includes mosaics and a superb amphitheater. The archaeological remains of Kourion - which was one of the island's most important city-kingdoms in antiquity - are of the most impressive on the island, and excavations have unearthed many significant finds, which can be viewed at the site. The magnificent Greco-Roman theatre - the site's centrepiece - was built in the 2<sup>nd</sup> century BC and extended in the 2<sup>nd</sup> century AD. The theatre has been restored, and is now used for open-air musical and theatrical performances - mainly during the summer months - making it one of the most popular settings for high-caliber cultural events. From this beautiful, unspoiled spot perched high on a cliff, we will enjoy the dazzling view of the ruins and the sea below.

Participants interested in spending some relaxing free time at the nearby Kourion beach have the option to skip the archaeological tour. For more information contact the Registration desk.







### 20:00-22:30 – Gala Dinner at Evagoras Lanitis Centre - Carob Mill

The Evagoras Lanitis Cultural Centre is located in the centre of the old town of Limassol, between the Medieval Castle and the New Limassol Marina. It comprises one third of the Carob Mill, which is one of the largest industrial building in Cyprus. This area of the building was originally used for the storage of Carob products, which were processed through the carob crushers. The milling equipment is situated in the central bay of the building and has been restored as a carob museum. Dinner will be served in the Carob Mill Richard & Berengaria Ballroom where participants will enjoy a beautiful dinner, with music and dancing, and superb opportunities for networking in a relaxed environment.

The first bus will depart at 22:30. Later departure will be available.



# Local Map



C.T.O Tourist Information:

- Restaurant / Tavern
- Cafe / Bar / Cafe
- Nightlife
- Shopping
- Bank / ATM
- Petrol Station
- Church
- Municipal parking Place
- Beach
- Cycling Station

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